In the Claims:

This listing of claims replaces all prior versions.

1. (*Currently Amended*) A frequency-domain decision feedback equalizer device for single carrier modulation comprising:

a first section configured to generate an output signal and including

a fast Fourier transformation circuit configured to perform a fast Fourier transformation on a first vector of signals inputted into said first section, and outputting a second vector of signals,

a feed forward equalizer circuit configured and coupled to perform feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters, and outputting a third vector of signals, and

an inverse fast Fourier transformation circuit configured and coupled to perform an inverse fast Fourier transformation on said third vector of signals, and outputting a fourth vector of signals; and

a second section including

a feedback filter circuit configured and coupled to perform linear filtering of a signal derived from an output signal of said second section,

an adder circuit coupled to add the output signal of said feedback filter circuit to the output signal of said first section, and

a detector circuit configured and coupled to receive the output signal of said adder circuit and generate said output signal of said second section by extracting samples from the output signal of said adding means.

2. (*Previously presented*) The device according to claim 1, wherein said feed forward equalizer circuit generates equalization parameters adapted for minimizing the signal-to-noise ratio of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section.

3. (*Previously presented*) The device according to claim 1, wherein said feed forward equalizer circuit generates equalization parameters by taking into account a fast Fourier transformation

estimation of a channel impulse response of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section.

4. (*Previously presented*) The device according to claim 1, wherein said first section further comprises:

a serial to parallel converter circuit coupled to convert a sequence of signals input into said first section to said first vector of signals, and

a parallel to serial converter circuit coupled to convert said fourth vector of signals to a sequence of output signals of said first section.

5. (*Previously presented*) The device according to claim 4, wherein said serial to parallel converter circuit is adapted to receive scalar signals.

6. (*Previously presented*) The device according to claim 4, wherein said serial to parallel converter circuit generates said first vector of signals including blocks of a predetermined number of consecutive samples of the signals input into said first section.

7. (*Previously presented*) The device according to claim 4, wherein said parallel to serial converter circuit and said feedback filter means are configured to output scalar signals.

8. (*Previously presented*) The device according to claim 6, wherein said parallel to serial converter circuit is configured to output a scalar signal which is constituted by consecutive blocks of a predetermined number of samples, each block being built with the predetermined number of samples of each block of said fourth vector of signals.

9. (*Previously presented*) The device according to claim 1, wherein said detector circuit is configured to receive and output discrete time signals.

10. (*Currently Amended*) The device according to claim 1, wherein said detector circuit is configured to generate said output signal of the second section.

11. (*Previously presented*) The device according to claim 1, wherein said second section further comprises a feedback input generator for receiving said output signal of said second section and providing an output signal which is built by consecutive blocks, each block including first a pseudo noise sequence and second a predetermined number (M) of samples from said output signal of said section, to said feedback filter circuit.

12. (*Previously Presented*) The device according to claim 1, further including a receiver of a communication system using a single carrier modulation, wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device.

Claims 13-16 (*Cancelled*).

17. (*Previously presented*) The device according to claim 1, further including a communication system including a transmitter using a single carrier modulation, for transmitting data, comprising a modulator circuit configured to organize the data in blocks wherein each block is separated by a sequence of a predetermined signal and a receiver of a communication system using a single carrier modulation, wherein said receiver includes said first and second sections of the frequency-domain decision feedback equalizer device.

18. (*Currently Amended*) A frequency-domain decision feedback equalizing method for single carrier modulation, preferably for use in a broadband communication system, comprising the steps of:

in a first section providing an output signal of said first section by:

performing a fast Fourier transformation on a first vector of signals inputted, and as a result providing a second vector of signals,

performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters, and as a result providing a third vector of signals,

performing an inverse fast Fourier transformation on said third vector of signals, and as a result providing a fourth vector of signals, and

providing an output signal of said first section on the basis of said fourth vector of signals; and

in a second section:

performing a linear feedback filtering of a signal derived from an output signal of said second section, and providing a filtered signal,

adding said filtered signal to said output signal of said first section, and providing an added signal, and

generating said output signal of said second section by extracting samples from said added signal.

19. (*Original*) The method according to claim 18, wherein in said feed forward equalization step equalization parameters are generated adapted for minimizing the signal-to-noise ratio of the signal processed, preferably in the output signal of said first section.

20. (*Previously Presented*) The method according to claim 18, wherein in said feed forward equalization step equalization parameters are generated by taking into account a fast Fourier transformation estimation of a channel impulse response of the signal processed, preferably in the output signal of said first section.

21. (*Previously Presented*) The method according to claim 18, comprising in said first section the further steps of:

serial to parallel converting a sequence of signals inputted into said first section to said first vector of signals, and

parallel to serial converting said fourth vector of signals to a sequence of output signals of said first section.

22. (*Original*) The method according to claim 21, wherein said serial to parallel converting step is provided to process scalar signals.

23. (*Previously presented*) The method according to claim 21, wherein said serial to parallel converting step is provided to generate said first vector of signals including blocks of a predetermined number of consecutive samples of the signals inputted into said first section.

24. (*Previously Presented*) The method according to claim 21, wherein said parallel to serial converting step and said linear feedback filtering step are provided to output scalar signals.

25. (*Previously Presented*) The method according to claim 23, wherein said parallel to serial converting step is provided to output a scalar signal which is constituted by consecutive blocks of a predetermined number of samples, each block being built with the predetermined number of samples of each block of said fourth vector of signals.

26. (*Previously Presented*) The method according to claim 18, wherein said extracting step in said second section is adapted to process discrete time signals.

27. (*Previously Presented*) The method according to claim 18, wherein said extracting step in said second section is provided to generate said output signal.

28. (*Previously Presented*) The method according to claim 18, comprising in said second section a feedback input generating step for processing said output signal of said second section and providing an output signal which is built by consecutive blocks, each block including first a pseudo noise sequence and second a predetermined number of samples from said output signal of said section, to said feedback filter means.

Claims 29-32 (*Cancelled*).

33. (*Previously presented*) A frequency-domain decision feedback equalizer device for single carrier modulation, the device comprising:

a first section including

a fast Fourier transformer to perform a fast Fourier transformation on a first vector of single carrier signals inputted into said first section, and to output the transformed signals as a second vector of signals,

a feed forward equalizer to perform a feed forward equalization by generating equalization parameters using a fast Fourier transformation estimation of a channel impulse response of an output single carrier signal of said first section, multiplying each of the components of said second vector of signals with the generated equalization parameters to reduce the signal-noise ratio of the signals, and outputting the multiplied signals as a third vector of signals, and

an inverse fast Fourier transformer to perform an inverse fast Fourier transformation on said third vector of signals, and to output the inversely transformed signals as a fourth vector of signals that is the output signal of the first section; and

a second section including

a feedback filter to linearly filter a signal derived from an output signal of said second section,

an adder to add the output signal of said feedback filter to the output signal of said first section, and

a detector to receive the output signal of said adder and generate said output signal of said second section by extracting samples from the output signal of said adder.

34. (*Previously presented*) The device according to claim 11, wherein:

the detector circuit is configured to receive and output discrete time signals selected from a constellation consisting of a set of symbols; and

wherein the pseudo noise sequence is constructed from symbols selected from the constellation.

35. (*Previously presented*) The device according to claim 11, wherein:

the detector circuit is configured to receive and output discrete time signals selected from a first constellation consisting of a set of symbols; and

wherein the pseudo noise sequence is a selected sequence constructed from symbols selected from a second constellation exclusive to the first constellation.

36. (*Previously presented*) The device according to claim 11, wherein:

the detector circuit is configured to output scalar signals including a number of samples consisting of the predetermined number (M) of consecutive samples; and

the feedback input generator is configured to output the pseudo noise sequence appended to the scalar signal.